RAJPUROHIT ANIL

Contact

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Languages

English
Hindi
Gujarati

Summary Professional Synopsis

FPGA Developer specializing in front end development of design . Experienced with all stages of the development cycle for dynamic projects. Well-versed in VHDL programming language and verification of IP using UVM methodology. Strong background in lt project management and FPGA design .

Skill Highlights

HDL Language	: Verilog HDL
EDA synthesis Tools	: Xilinx Vivado , Altera Quartus II
EDA Verification Tools	: Mentor's ModelSim, QuestaSim, **Synopsys VCS**
Methodology	: UVM
Debugging tool	: SignalTap II Logic analyzer

Experience

1. **Hp pps global soft pvt ltd Bangalore .**
   Role:FPGA Developer
   Duration: March-2019-Present
   - Role include FPGA design for HP printer .
   - RTL design of printer's Pen and implementation of test bench for the same .
   - Quality analysis and testing of product .
   - Integration of the product at system level.

2. **Numascale India Pvt. Ltd. Ahmedabad.**
   Role:ASIC DESIGN ENGINEER
   Duration: Sept 2018-Feb 2019
   - Worked on IP level Verification in System Verilog and UVM.
   - Worked on the Block level design using Verilog .
   - My role include IP verification and verification infrastructure improvement.
   - Involved in writing/updating test case to verify IP, updating, writing functional coverage.

3. **Sandeepani School Of Embedded Design Bangalore.**
   Role:TRAINEE ENGINEER
   Duration: Nov 2017- May 2018
   - Had hands on experience on FPGA design tool by Xilinx.
   - Worked on block level IP Verification using System Verilog and UVM.
   - RTL design in Verilog using QuestaSim

4. **Megachip Instrumentation Pvt. Ltd. Bangalore.**
   Role:APPRENTICE SERVICE ENGINEER
   Duration: Aug 2016- Apr 2017
   - My role include TOSHIBA CT SCAN service of single slice , 4 Slice and 16 Slice Toshiba Machine installation and service.
   - Performed Circuit debugging and Resolved the issue in Electronics circuits.

Education

- **B.E.** in Electronics & communication From Acharya Institute of Technology (V.T.U.) in 2016 with 60.34 %.
- **10+2** (Intermediate) in Vidya Bharti Public School From R.B.S.E. in 2010 with 65.54 %.
- **S.S.L.C**. in Senior Secondary School, Ratan-nagar, Churu From R.B.S.E. in 2008 with 74.50 %.

Certification

Professional development course in VLSI Design and Verification from CoreEl Technologies(I) Pvt. ltd Bangalore, India .